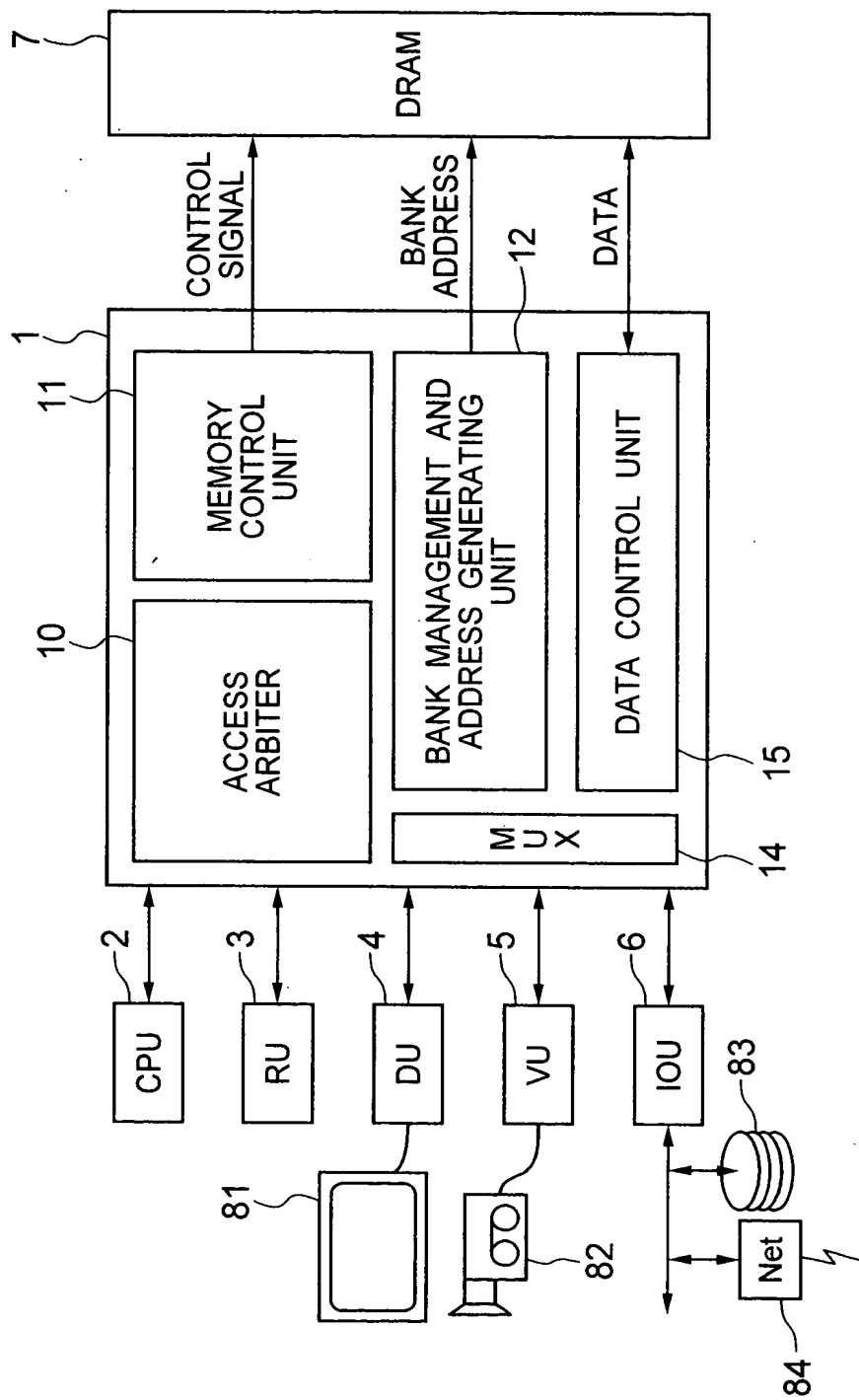


FIG. 1



# FIG. 2

COLUMN ADDRESS							LINE		
BANK ADDRESS : 0	0	1	2	...	31	2	...	510	511
ROW ADDRESS : 0	0	1	2	...	31	2	...	510	511
BANK ADDRESS : 0	0	1	2	...	31	2	...	510	511
ROW ADDRESS : 0	:	:	:	...	:	:	...	:	:
BANK ADDRESS : 0	0	1	2	...	31	2	...	510	511
ROW ADDRESS : n	0	1	2	...	31	2	...	510	511
BANK ADDRESS : 1	0	1	2	...	31	2	...	510	511
ROW ADDRESS : n	0	1	2	...	31	2	...	510	511
BANK ADDRESS : 2	:	:	:	...	:	:	...	:	:
ROW ADDRESS : n	:	:	:	...	:	:	...	:	:

# FIG. 3

COLUMN ADDRESS					LINE				
0	1	2	...	31	0	1	2	...	31
32	33	34	...	63	32	33	34	...	63
64	65	66	...	95	64	65	66	...	95
BANK ADDRESS : 0 ROW ADDRESS : 0					BANK ADDRESS : 1 ROW ADDRESS : 0				
496	497	498	...	511	496	497	498	...	511
BANK ADDRESS : 1 ROW ADDRESS : m					BANK ADDRESS : 2 ROW ADDRESS : m				
BANK ADDRESS : 2 ROW ADDRESS : n					BANK ADDRESS : 3 ROW ADDRESS : m				
BANK ADDRESS : 2 ROW ADDRESS : n					BANK ADDRESS : 3 ROW ADDRESS : m				
BANK ADDRESS : 2 ROW ADDRESS : n					BANK ADDRESS : 3 ROW ADDRESS : m				

# FIG. 4

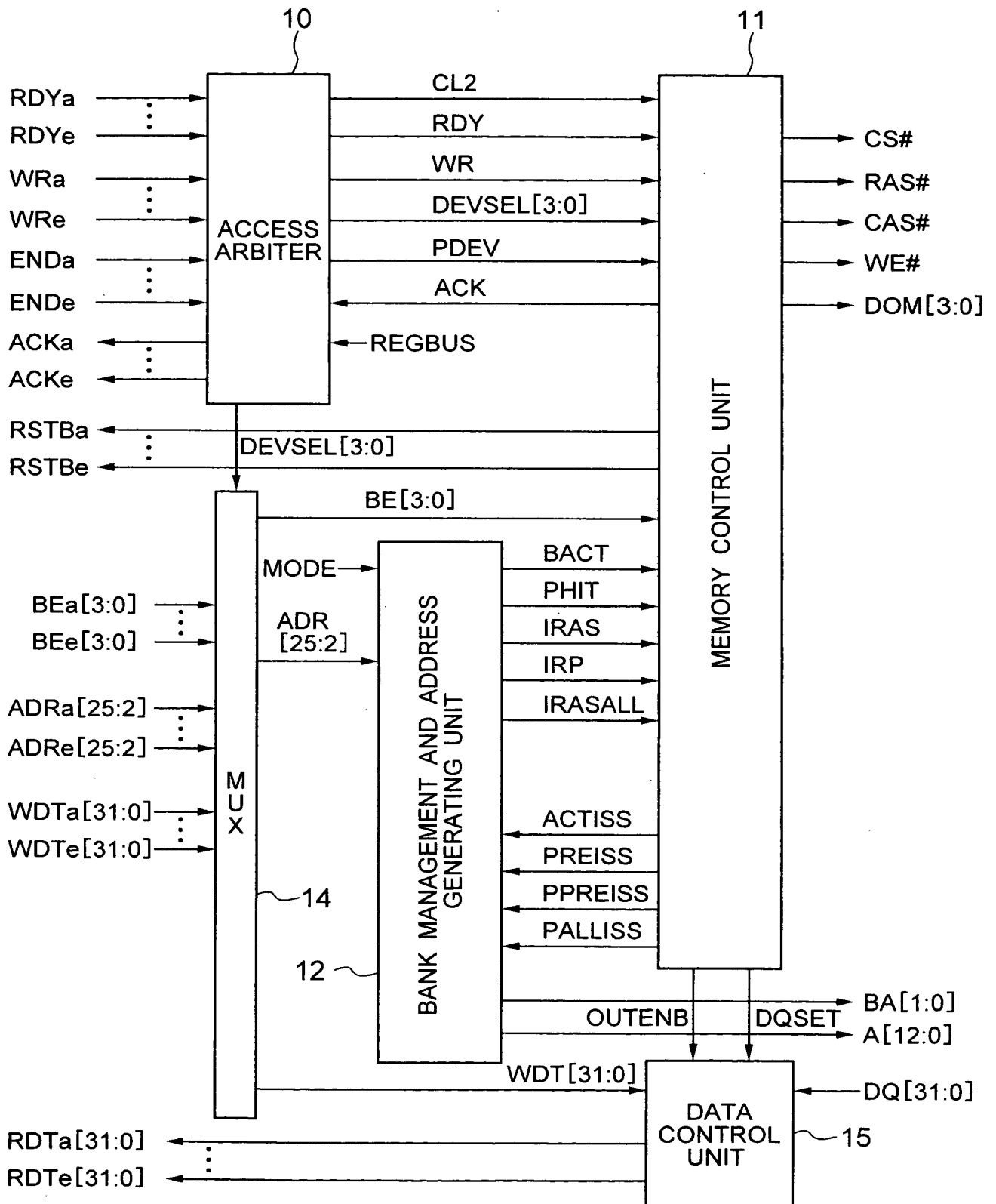


FIG. 5

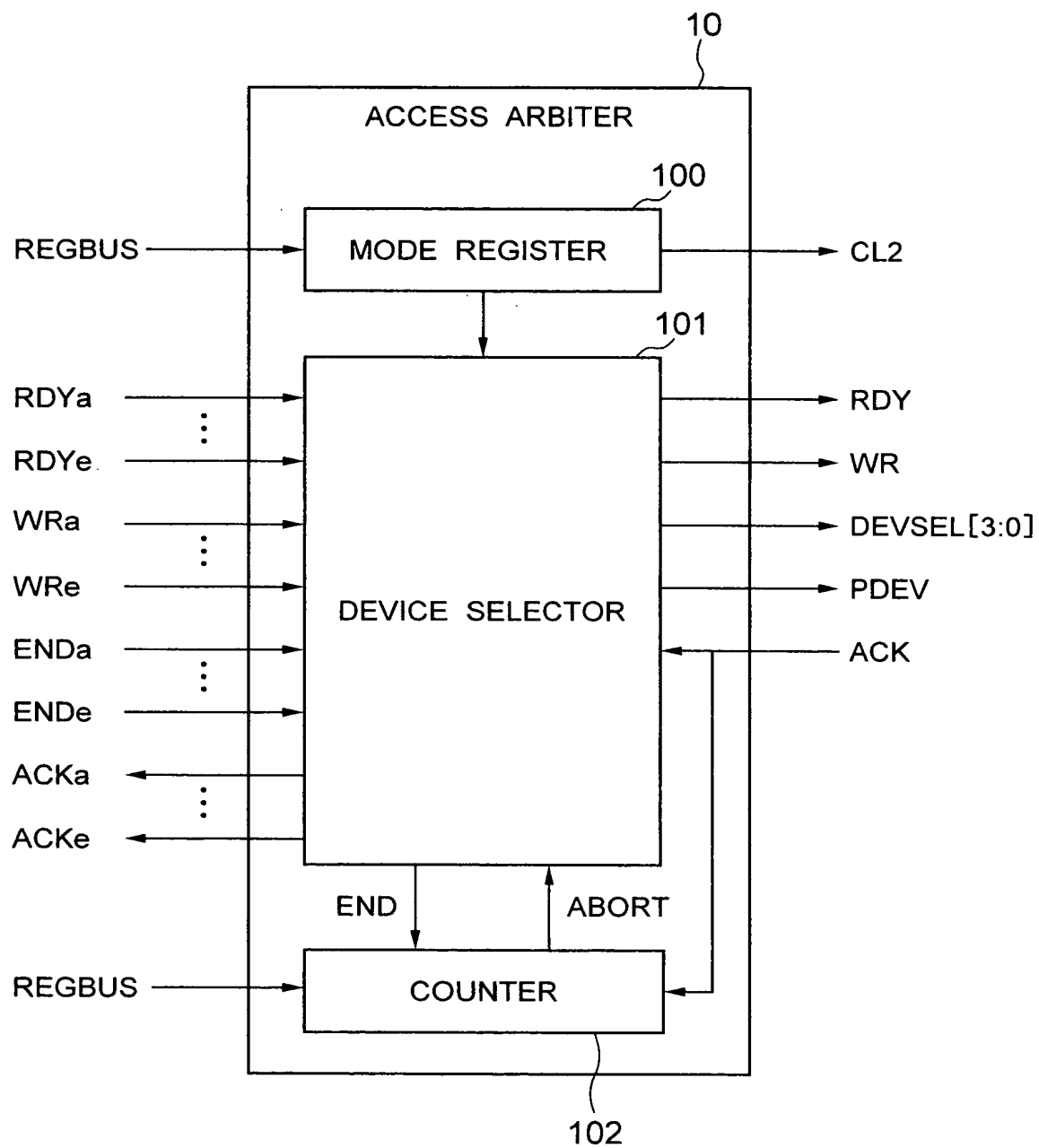



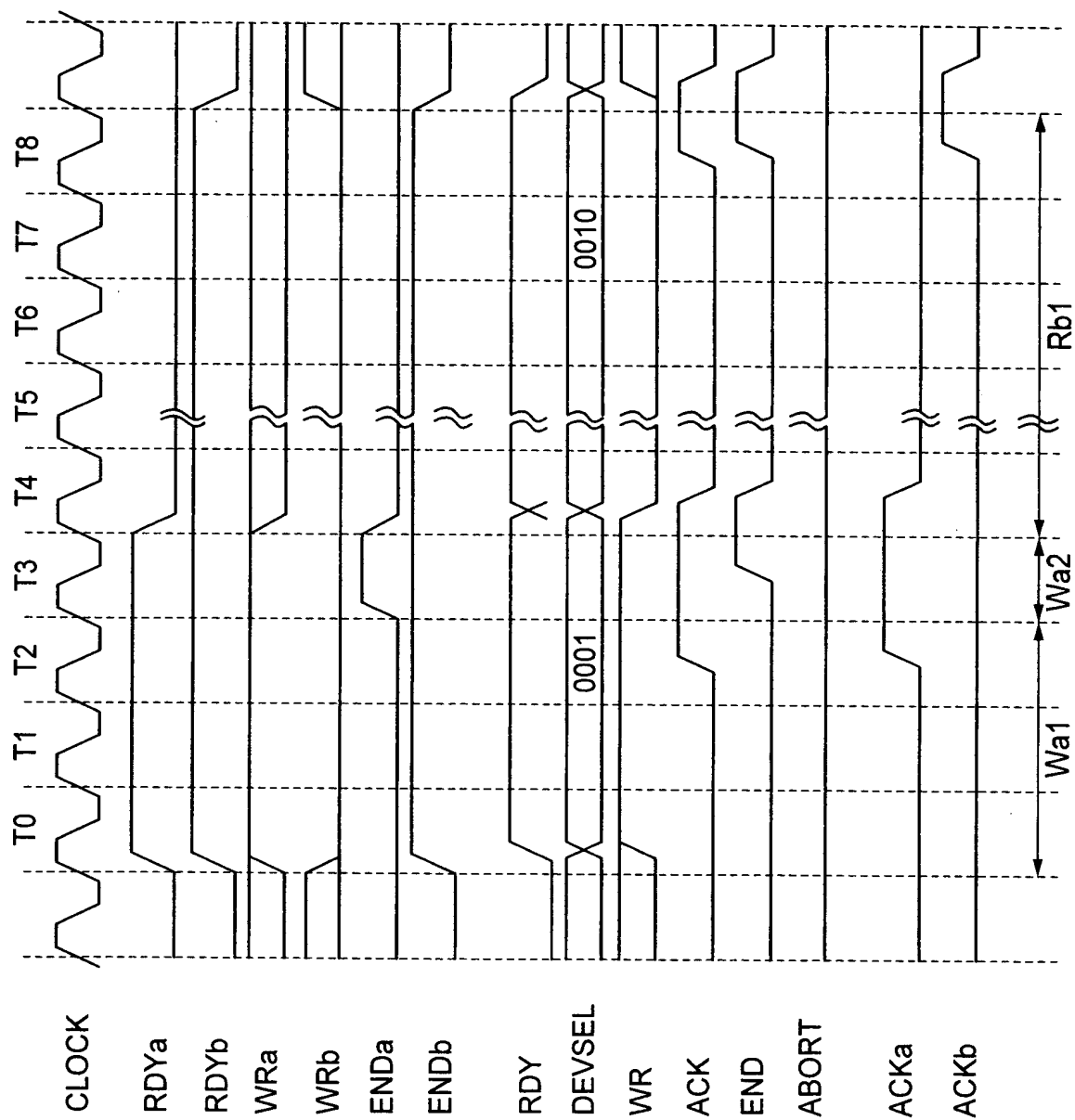
FIG. 6

MODE REGISTER		PRa[2:0]		PRb[2:0]		PRc[2:0]		PRd[2:0]		PRe[2:0]		CL2		PDa		PDb		PDc		PDd		PDe	
SETTING EXAMPLE :		000		001		010		011		010		1		0		1		0		0		1	

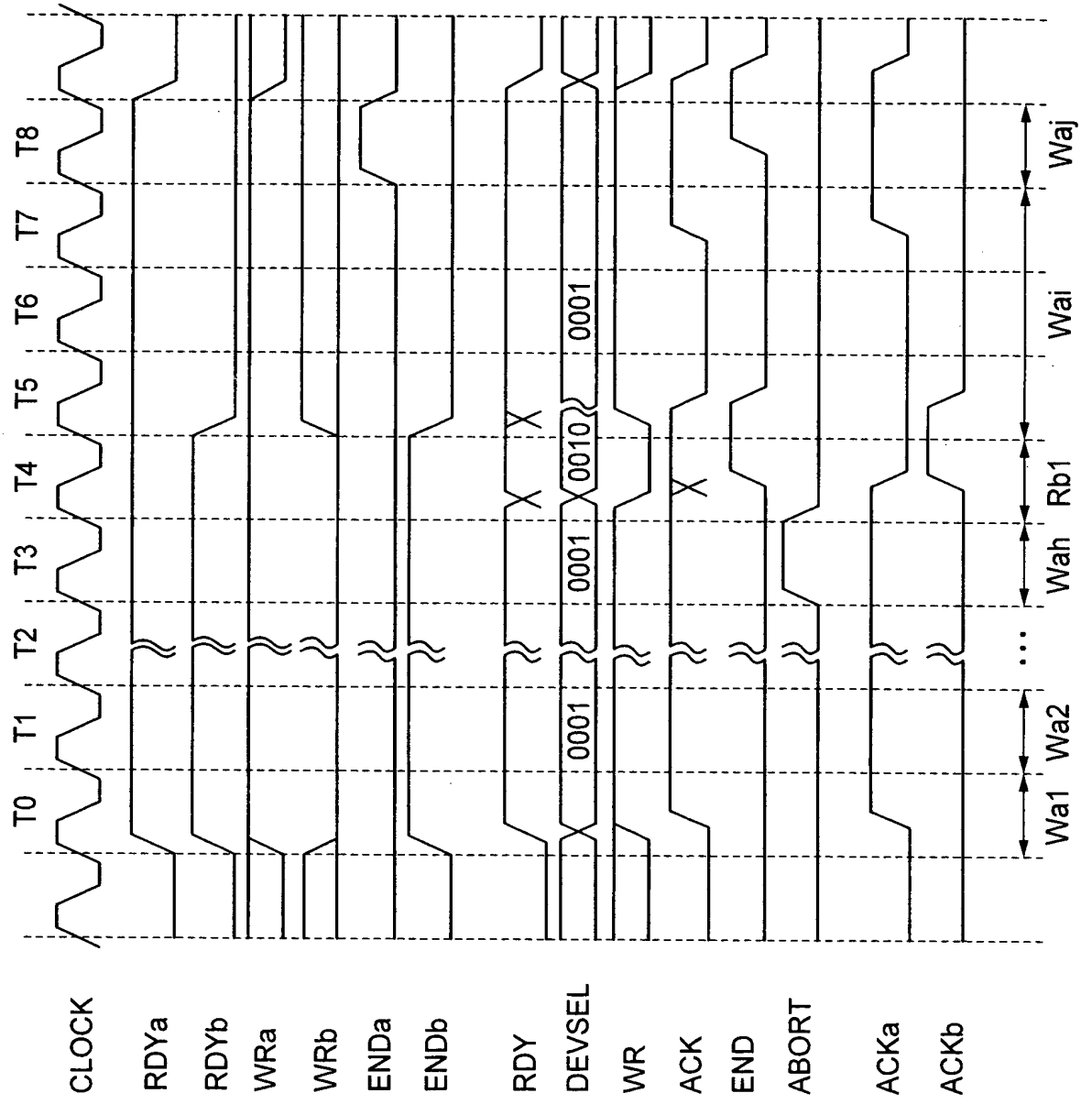
FIG. 7

Pri[2:0]	PRIORITY
000	PRIVILEGE MODE
001	PRIORITY : HIGH
010	
011	
100	
101	
110	
111	PRIORITY : LOW

# FIG. 8



# FIG. 9





# FIG. 10

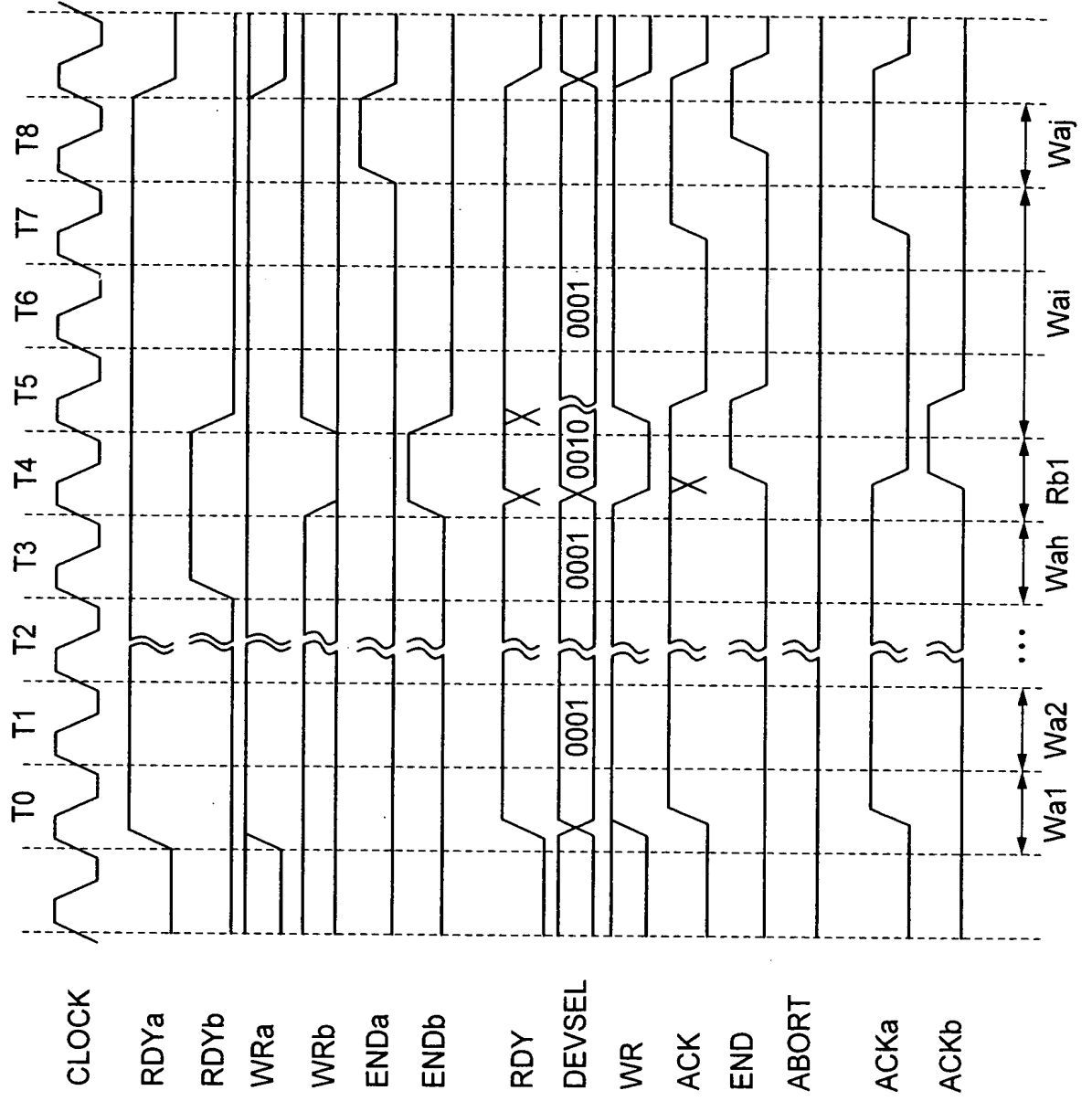


FIG. 11

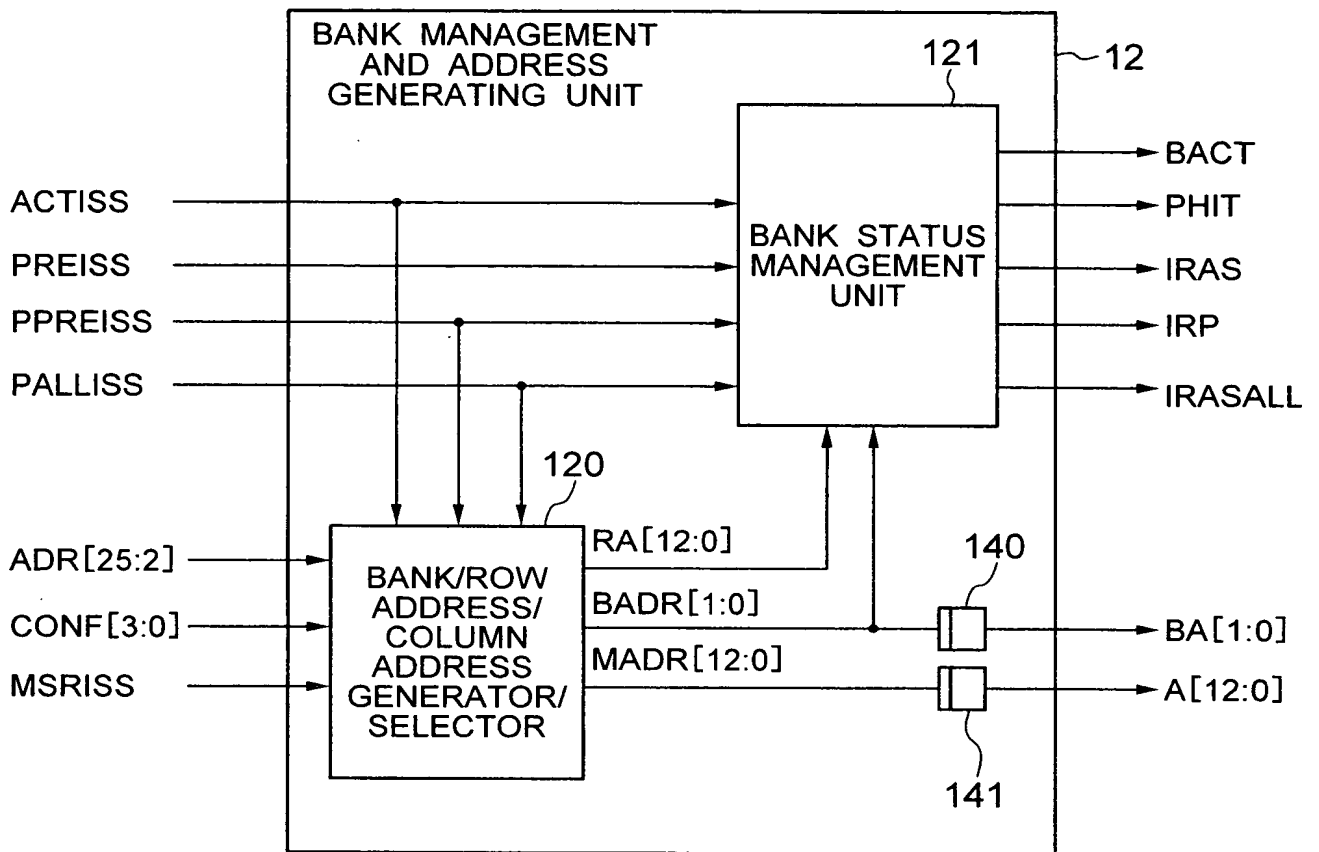
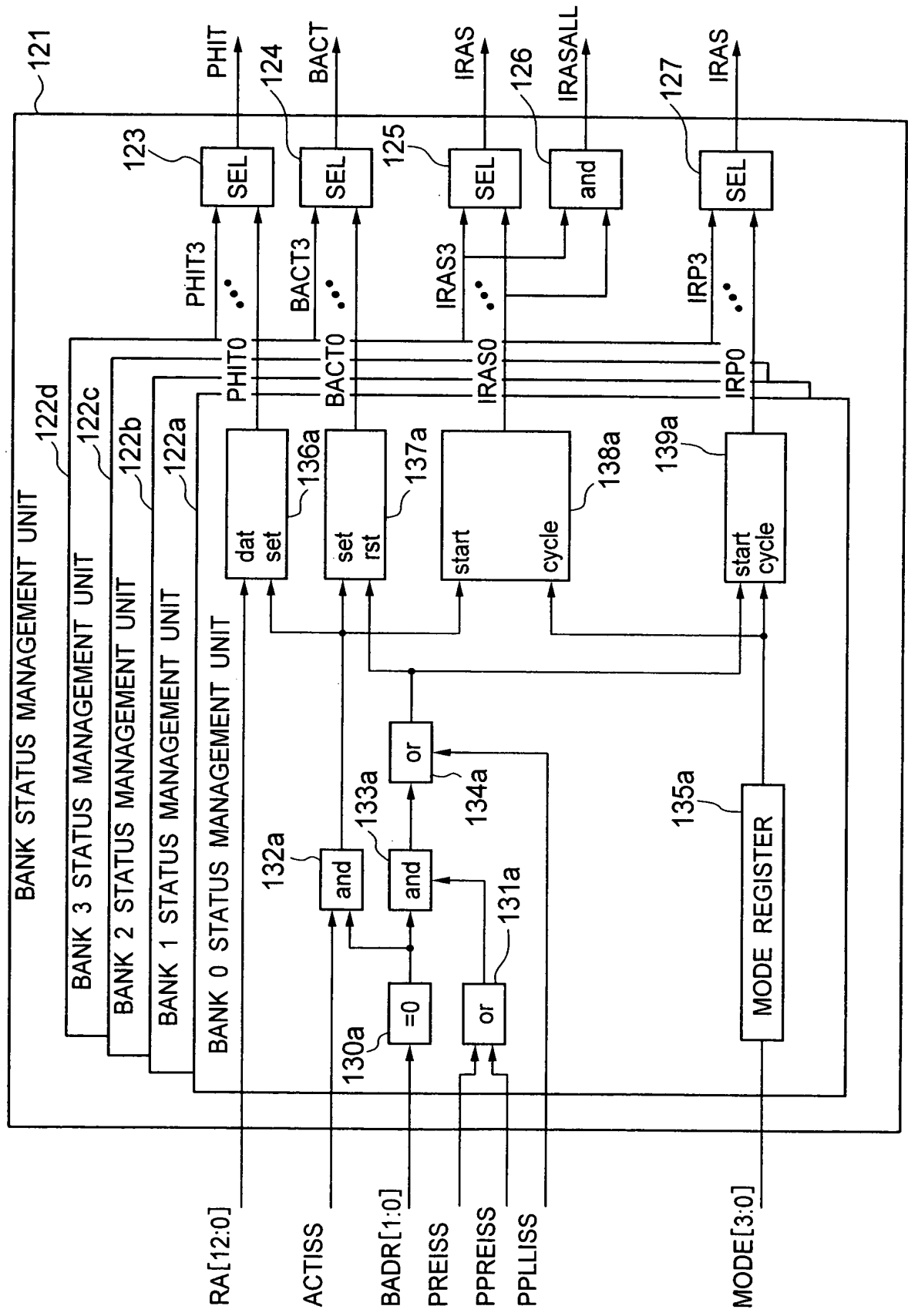


FIG. 12

CONF [3:0]	ACTISS	PPREISS	PALLISS	BADR[1:0]	RA[12:0]	MADR[12:0]
0	0	0	0	ADR[11:10]	{0, ADR[23:12]}	{00000, ADR[9:2]}
	1	0	0			{0, ADR[23:12]}
	0	1	0	ADR[11:10]+1		{00000, ADR[9:2]}
	0	0	1	ADR[11:10]		{00100, ADR[9:2]}
1	0	0	0	ADR[12:11]	{0, ADR[24:13]}	{0000, ADR[10:2]}
	1	0	0			{0, ADR[23:12]}
	0	1	0	ADR[12:11]+1		{0000, ADR[10:2]}
	0	0	1	ADR[12:11]		{0010, ADR[10:2]}
2	0	0	0	ADR[12:11]	ADR[25:13]	{0000, ADR[10:2]}
	1	0	0			{0, ADR[23:12]}
	0	1	0	ADR[12:11]+1		{0000, ADR[10:2]}
	0	0	1	ADR[12:11]		{0010, ADR[10:2]}

# FIG. 13



# FIG. 14

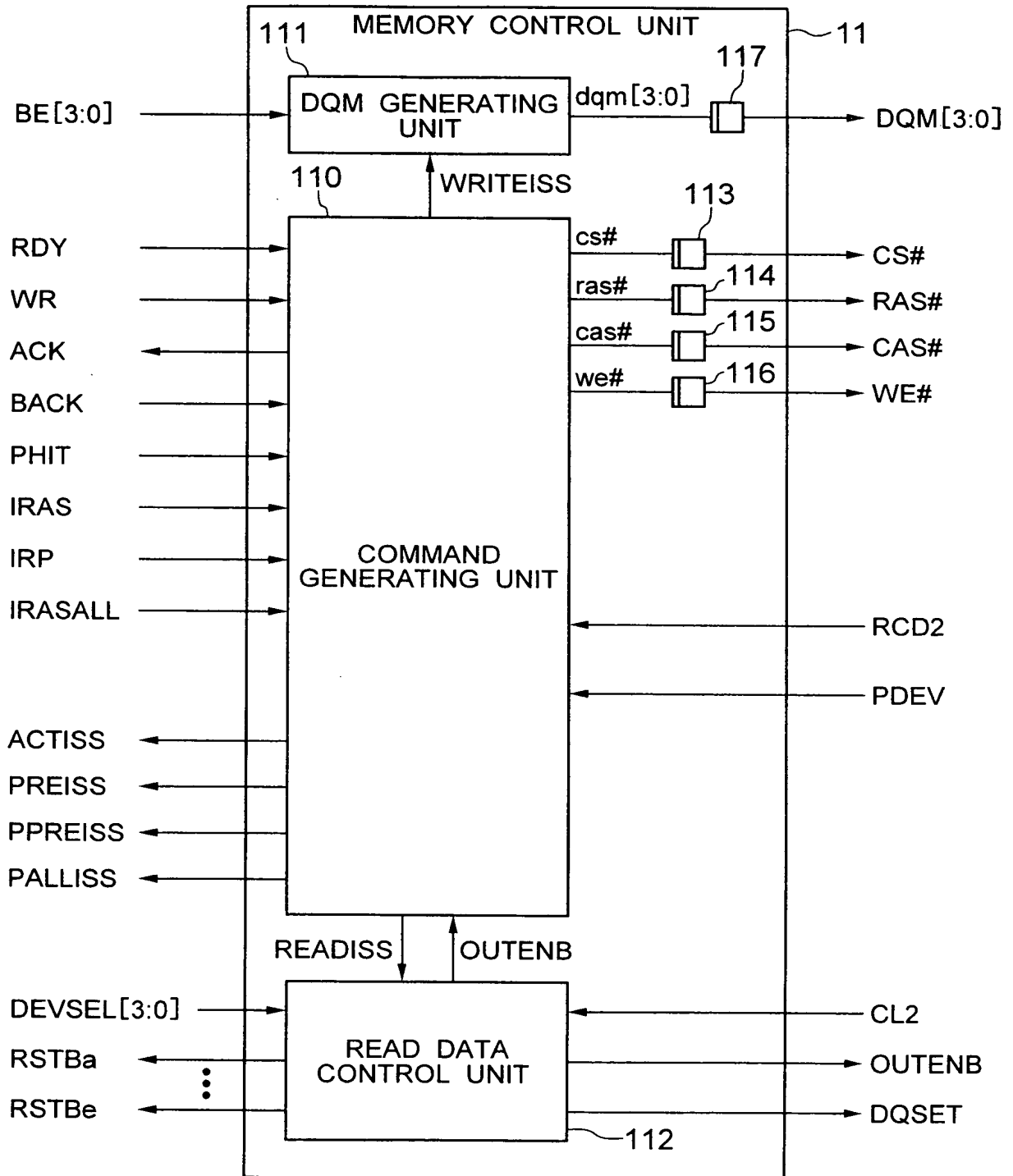
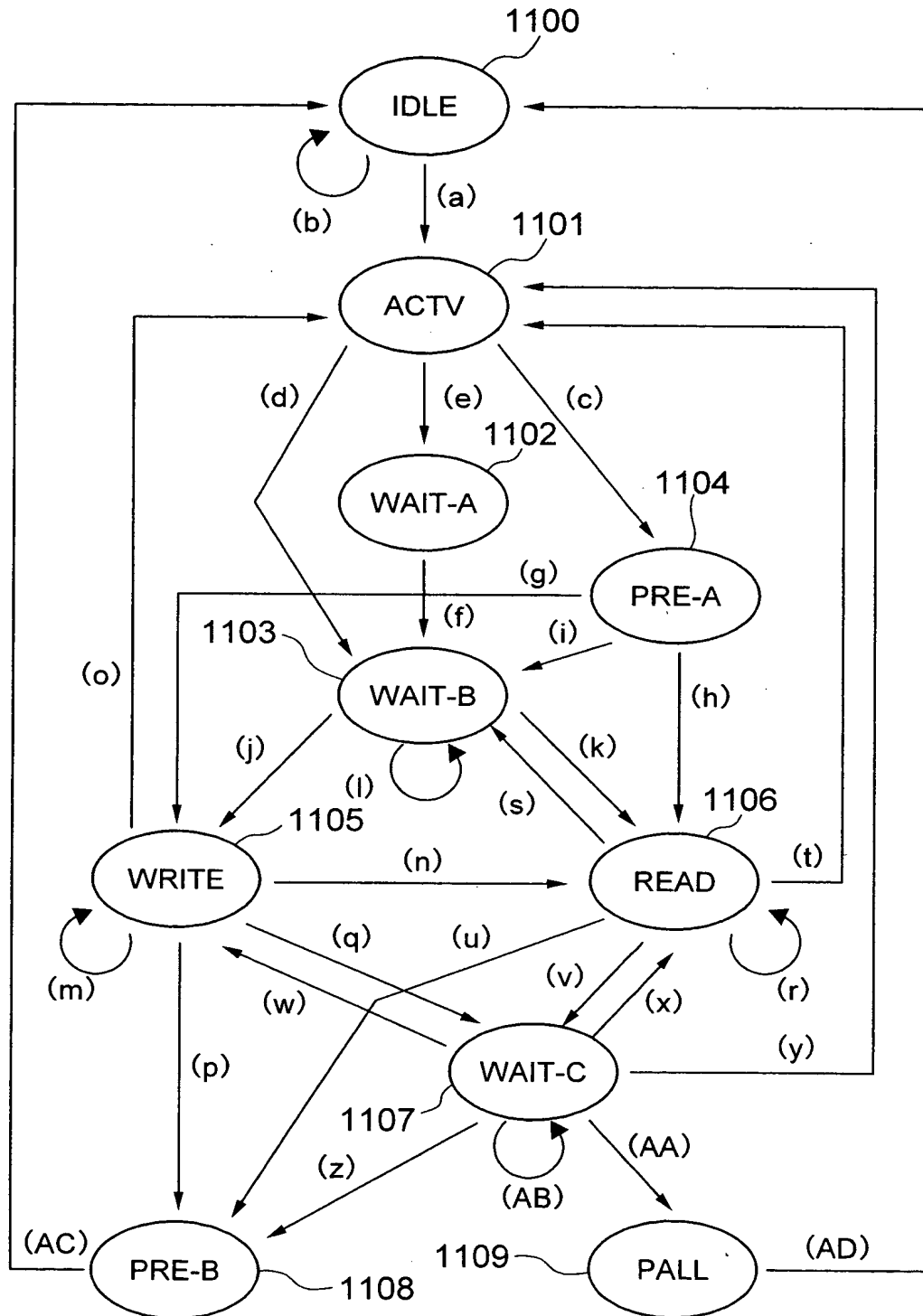


FIG. 15



# FIG. 16

#	TRANSITION SOURCE	TRANSITION DESTINATION	TRANSITION CONDITIONS
a	IDLE	ACTV	RDY & $\bar{\text{IRP}}$
b	IDLE	IDLE	(otherwise)
c	ACTV	PRE-A	PDEV
d	ACTV	WAIT-B	$\bar{\text{PDEV}}$ & RCD2
e	ACTV	WAIT-A	(otherwise)
f	WAIT-A	WAIT-B	(everything)
g	PRE-A	WRITE	CL2 & WR & OUTENB
h	PRE-A	READ	CL2 & $\bar{\text{WR}}$
i	PRE-A	WAIT-B	(otherwise)
j	WAIT-B	WRITE	WR & OUTENB
k	WAIT-B	READ	RDY & $\bar{\text{WR}}$
l	WAIT-B	WAIT-B	(otherwise)
m	WRITE	WRITE	RDY & PHIT & WR
n	WRITE	READ	RDY & PHIT & $\bar{\text{WR}}$
o	WRITE	ACTV	RDY & $\bar{\text{PHIT}}$ & $\bar{\text{BACT}}$ & IRP
p	WRITE	PRE-B	RDY & $\bar{\text{PHIT}}$ & BACT & IRAS
q	WRITE	WAIT-C	(otherwise)
r	READ	READ	RDY & PHIT & $\bar{\text{WR}}$
s	READ	WAIT-B	RDY & PHIT & WR
t	READ	ACTV	RDY & $\bar{\text{PHIT}}$ & $\bar{\text{BACT}}$ & IRP
u	READ	PRE-B	RDY & $\bar{\text{PHIT}}$ & BACT & IRAS
v	READ	WAIT-C	(otherwise)
w	WAIT-C	WRITE	RDY & PHIT & WR & $\bar{\text{OUTENB}}$
x	WAIT-C	READ	RDY & PHIT & $\bar{\text{WR}}$
y	WAIT-C	ACTV	RDY & $\bar{\text{PHIT}}$ & $\bar{\text{BACT}}$ & IRP
z	WAIT-C	PRE-B	RDY & $\bar{\text{PHIT}}$ & BACT & IRAS
AA	WAIT-C	PALL	$\bar{\text{RDY}}$ & IRASALL
AB	WAIT-C	WAIT-C	(otherwise)
AC	PRE-B	IDLE	(everything)
AD	PALL	IDLE	(everything)

# FIG. 17

TRANSITION DESTINATION STATUS	OUTPUT SIGNAL										
	ACK	ACTISS	PREISS	PPREISS	PALLISS	WRITEISS	READISS	cs#	ras#	cas#	we#
IDLE	0	0	0	0	0	0	0	1	1	1	1
ACTV	0	1	0	0	0	0	0	0	0	1	1
WAIT-A	0	0	0	0	0	0	0	0	1	1	1
WAIT-B	0	0	0	0	0	0	0	0	1	1	1
PRE-A	0	0	0	1	0	0	0	0	0	1	0
WRITE	1	0	0	0	0	1	0	0	1	0	0
READ	1	0	0	0	0	0	1	0	1	0	1
WAIT-C	0	0	0	0	0	0	0	0	1	1	1
PRE-B	0	0	1	0	0	0	0	0	0	1	0
PALL	0	0	0	0	1	0	0	0	0	1	0

# FIG. 18

WRITEISS	OUTPUT SIGNAL			
	DQM3	DQM2	DQM1	DQM0
0	0	0	0	0
1	$\overline{\text{BE}}[3]$	$\overline{\text{BE}}[2]$	$\overline{\text{BE}}[1]$	$\overline{\text{BE}}[0]$



# FIG. 19

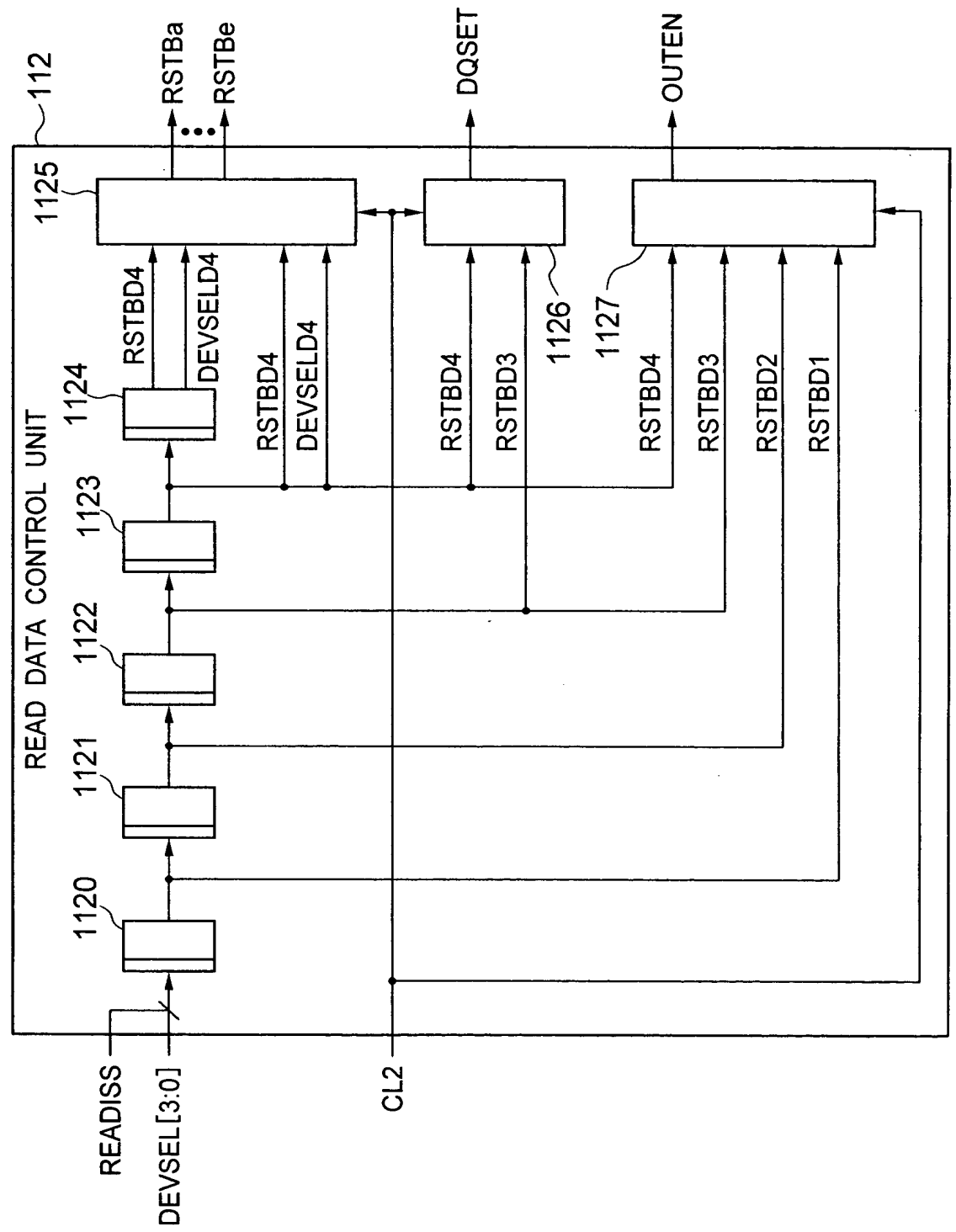


FIG. 20

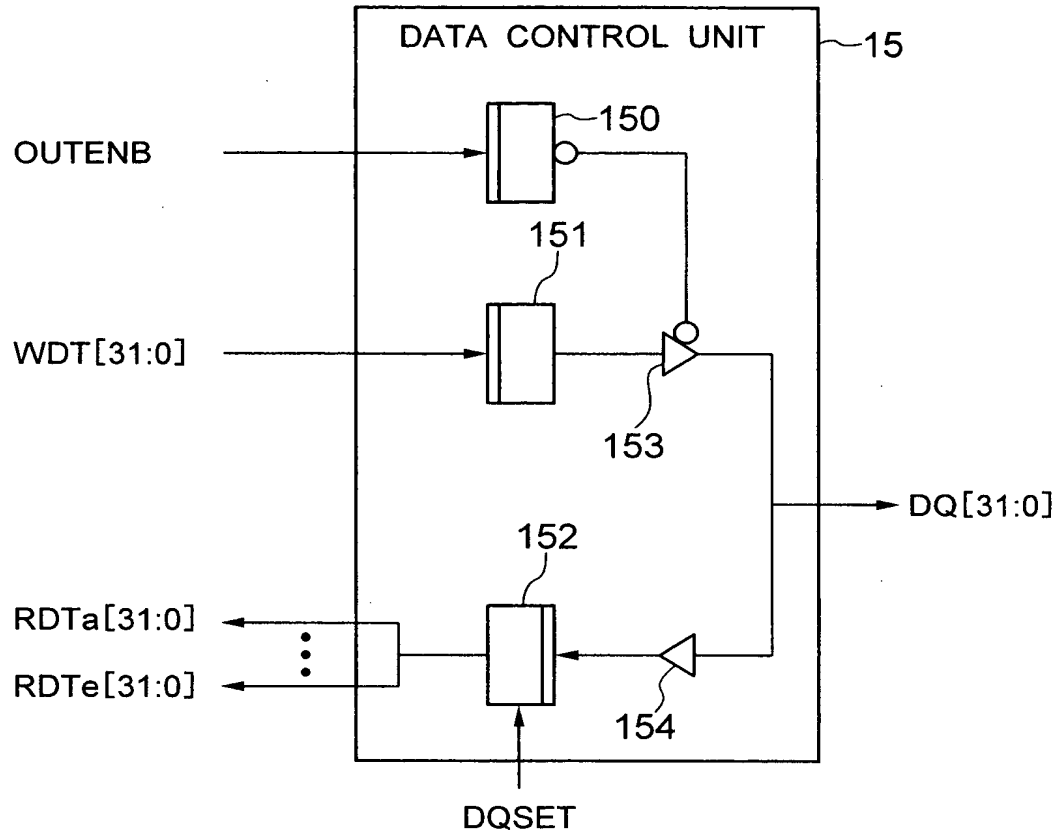
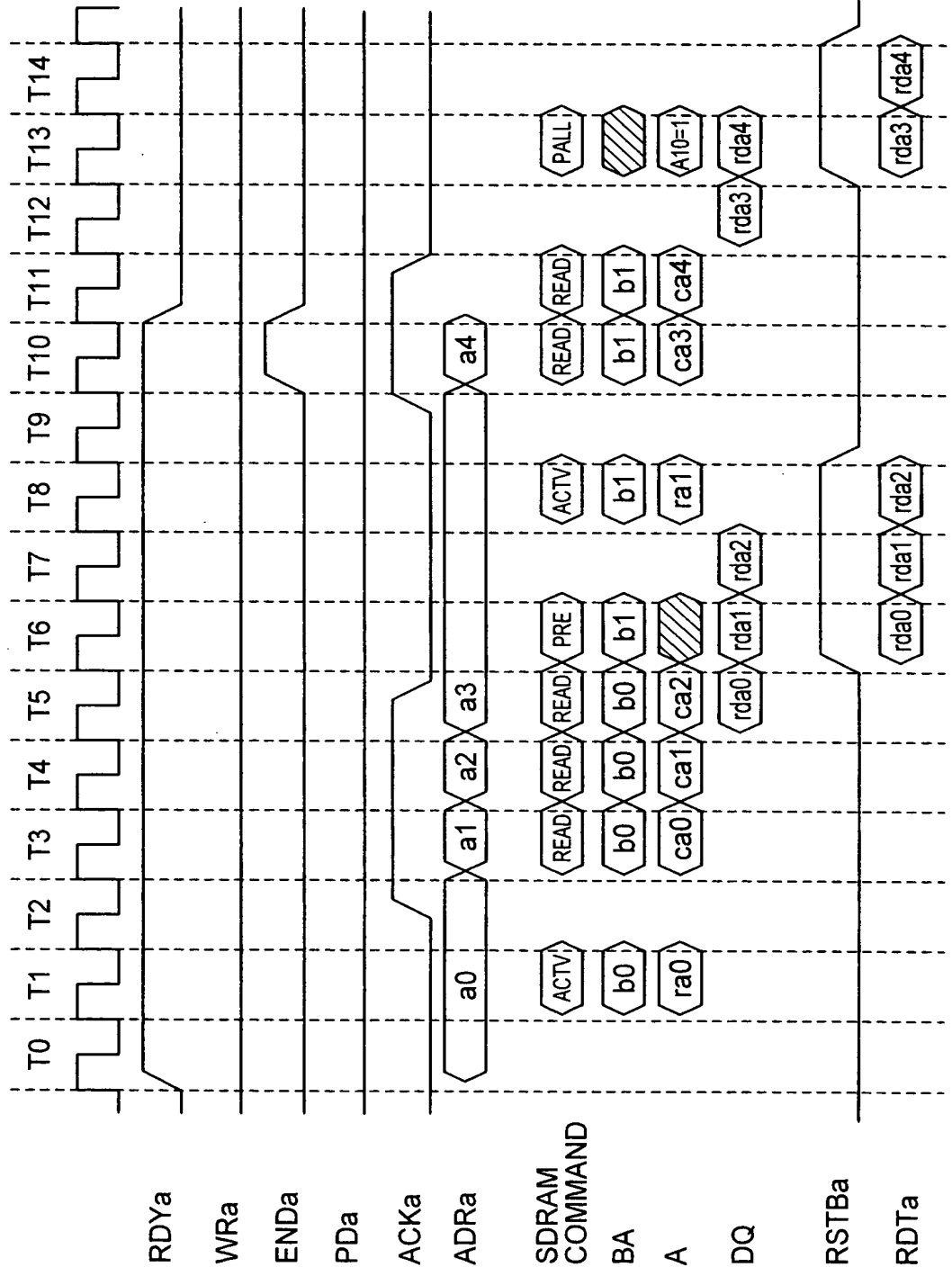


FIG. 21



# FIG. 22

